Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An apparatus for testing a variety of circuit boards ~~for use in a complex electronic device such as a multiprocessor computer system platform, said variety of circuit boards all~~ having ~~connectors~~ at least one connector compatible to a mating connector of said apparatus wherein said variety of circuit boards have potentially unlike circuit configurations, said apparatus ~~for testing~~ comprising:

a host computer with software for employing test vector files to ~~generate and programmably operate~~ perform scan testing on VLSI components ~~on~~ of a circuit board ~~connected to said apparatus for testing~~,

a distributed power supply configured to provide ~~providing~~ a ~~programmable~~ plurality of ~~programmable~~ voltage value outputs ~~contemporaneously~~ from a single power input to ~~said~~ a circuit board ~~connected to said apparatus for testing~~,

a logic card having maintenance circuitry ~~needed by the circuit board connected to said apparatus for testing~~ for connecting to ~~maintenance accessible circuitry on~~ ~~said~~ a circuit board ~~connected to said apparatus for testing~~,

~~programmable~~ at least one clock ~~clocks~~ for providing ~~on/off, slow, or static~~ clock signals, and

a mating connector for connecting ~~said~~ a circuit board ~~compatible connector~~ to said apparatus ~~for testing, for connecting said clock signals, said logic card~~

~~maintenance circuitry, and said power supply therethrough.~~ .

2. (Currently Amended) The apparatus of claim 1 further comprising programmable functional speed clocks to provide functional speed clock signals for at speed testing, said functional speed clock signals ~~also~~ ~~connectable~~ being connected through said mating connector to said variety of circuit boards.

3. (Original) The apparatus of claim 1 further comprising clock detectors for detecting clock signals received from said variety of circuit boards through said mating connector.

4. (Original) The apparatus of claim 1 further comprising general I/O pin connection detectors for detecting general I/O connections with said variety of circuit boards through said mating connector.

5. (Currently Amended) The apparatus of claim 1 wherein said mating connector has a plural-staged connect configuration wherein a first stage provides guides for initial insertion to a generally correct position and a sensor to determine when said generally correct position has been achieved, a second stage of which provides for establishment of an electrical connection to ~~said~~ a circuit board connected to said mating connector of said apparatus ~~for testing~~ and a sensor to determine when said electrical connection to ~~said~~ a circuit board has been achieved, and a third stage of which provides for electrical continuity testing to determine that electrical continuity has been achieved prior to a final stage of activation of any testing of circuitry of the circuit board connected to said apparatus ~~for testing~~, and wherein no later stage of said plural stages is accessible unless each earlier stage has been completed.

6. (Original) The apparatus of claim 5 wherein said final stage of testing comprises two stages, a static testing stage and a subsequent dynamic testing stage.

7. (Currently Amended) The apparatus of claim 5 wherein said mating connector has two apertures through which a light travels to two sensors, and wherein complete insertion of ~~said~~ a circuit board blocks said two apertures in a way to inhibit sensing from said two sensors when a ~~said~~ circuit board is inserted therein.

8. (Original) The apparatus of claim 7 wherein said two apertures are at one end of said mating connector forming a center-to-center axis substantially perpendicular to a mating axis of travel of said compatible connector when mating to said mating connector.

9. (Currently Amended) The apparatus of claim 7 wherein said second stage is not available unless said light ~~source~~ is blocked by a ~~said~~ circuit board.

10. (Currently Amended) The apparatus of claim 5 wherein ~~said tester~~ the apparatus is interfaced to ~~said~~ a circuit board through ~~a pogo pin/bed of nails~~ an interface driven against the circuit board by a pneumatic cylinder.

11. (Currently Amended) The apparatus of claim [[7]]10 wherein said pneumatic cylinder is driven by compressed air.

12. (Currently Amended) The apparatus of claim [[8]]10 wherein said ~~interfacing~~ interface is ~~designed~~ configured to handle on the order of ten

thousand insertions.

13. (Currently Amended) The apparatus of claim 6 ~~wherein said tester additionally has a series of three lights,~~ further comprising a red light, a yellow light and a green light, visible to an operator during operation of said plural staged connect configuration, and wherein said red light is visible until said initial insertion to a generally correct position is accomplished, and wherein said yellow light is visible until said establishment of said electrical connection to said apparatus ~~for testing~~, and wherein after said third stage is accomplished and continuity testing has occurred satisfactorily, said green light becomes visible.

14. (Currently Amended) The apparatus of claim 1 further comprising a scanner for reading an optically encoded identifier on ~~said~~ a circuit board connected to said apparatus ~~for testing~~ as [[it]]the circuit board is being connected to said apparatus, and for sending a message to said computer identifying said circuit board connected to said apparatus ~~for testing as a particular model of circuit board among multiple models capable of being tested by said apparatus~~, and wherein said computer has multiple data sets, one for each model of a plurality of predetermined types of circuit boards and model identifier software for receiving said message and applying an appropriate one of said multiple data sets to said circuit board connected to said apparatus ~~for testing~~, consistent with said message.

15. (Currently Amended) The apparatus of claim [[1]]14 wherein said scanner is a bar code reader.

16. (Currently Amended) The apparatus of claim 1 wherein said apparatus ~~for testing~~ has two mating connectors for connection to two different types of

~~compatible connecters~~ circuit boards such that two different types of circuit boards can be tested on said apparatus.

17. (Original) The apparatus of claim 16 wherein said two mating connectors share common resources of said apparatus, including at least said power supply.

18. (Currently Amended) The apparatus of claim 17 wherein said common resources include ~~said~~ a host computer.

19. (Currently Amended) The apparatus of claim 17 wherein a first of said mating connectors is for connecting to a 64 bit wide address bus on ~~said~~ a first circuit board, and a second of mating said connectors is for connecting to a 32 bit wide address bus on ~~said~~ a second circuit board.

20. (Currently Amended) The apparatus of claim [[17]]19 wherein said distributed power supply connects to power circuitry on both of the first and second circuit boards ~~said 64 bit wide and said 32 bit wide circuit boards~~.

21. (Original) The apparatus of claim 1 wherein said host computer is substantially equivalent to a management processor component of said complex electronic device.

22. (Currently Amended) The apparatus of claim 21 wherein said host computer ~~has~~ includes a software facility for simulating circuit board TAP and Clock and Control Command facilities ~~useful~~ for formatting of ~~said~~ software data

into ~~said~~ test vector data to operate as a test vector appropriate to a logical register structure in ~~said~~ a circuit board.

23. (Original) The apparatus of claim 1 wherein said mating connector comprises a TAP interface.

24. (Currently Amended) The apparatus of claim 23 wherein test vectors are ~~deliverable~~ delivered through said TAP interface.

25. (Currently Amended) The apparatus of claim 1 wherein said host computer reports all errors in a format which identifies ~~identifying~~ physical errors to an operator.

26. (Currently Amended) The apparatus of claim 25 wherein said apparatus is associated with a printer for printing said reports identifying physical errors onto receipts physically ~~associatable~~ associated with a circuit board.

27. (Currently Amended) The apparatus of claim 26 wherein said apparatus runs software for constructing ~~said~~ the reports of said physical errors based on a same set of data files used to create a plurality of test vectors for a circuit board being tested.